

### MESSAGE FROM HoP, Prof Ricky Ang

Dear EPD family,  
 November marked an eventful month for EPD. We had a couple of workshops held at ARMS lab, industry site visits, industry and academic lectures as well as a Pillar Information Session for Freshmore students. 10 new projects were also launched by our 30.111 Entrepreneurship class on Kickstarter. We encourage and hope that our students, staff and faculty will continue this dynamic & innovative spirit and be engaged in our Pillar activities.

### UPCOMING EVENTS

30 Nov	1 Dec	2 Dec
EPD 3D Exhibition	EPD Faculty & Staff Team Building Event	Admissions & Career Talk



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### ACHIEVEMENTS & ANNOUNCEMENTS

- Congratulations to **EPD PhD student, Ezgi Sahin!** Ezgi was one out of ten students awarded the **Incubic/Milton Chang Grant** by Optical Society of America (OSA) Foundation. With this grant, Ezgi traveled to the "Frontiers in Optics" Conference in Washington D.C., where she presented two of her papers. One of her papers was also selected for the OSA Rapid Fire Oral Presentation.
- Congratulations to **EPD PhD student, George Chen!** George won 3<sup>rd</sup> position out of 55 participants in **Falling Walls Lab Competition** in Xi'an, China.
- Team STRIDER Pte. LTD. under SUTD Organisation of Autonomous Robots (SOAR) which comprises EPD students **Chen Bainian** and **Jason Swee** along with other SUTD students, won the Grand Prize in the **Tech Factor Challenge 2017**, worth \$25,000. Their solution was to convert existing walkers for the elderly into wheeled walkers in just 10 minutes, using special braking technology. Congratulations!



### FEATURED : REVERSIBLE VALLEYTRONIC COMPUTER BASED ON NOVEL DIRAC MATERIALS

EPD Authors – Yee Sin Ang (Postdoc), Professor Ricky L. K. Ang (PI), Assistant Professor Yang Shengyuan (Collaborator)

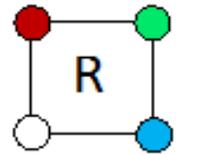
Valleytronics is an emerging device concept based on the manipulation of electron's quantum valley degree of freedom. In this work, by using the unusual physical properties of Dirac materials, we design versatile valleytronic logic gates capable of performing all 16 types of two-input Boolean logical operations and **logically-reversible computing**.

Traditional reversible logic gate generates wasteful garbage and ancilla bits in maintaining logical-reversibility. As inspired by EPD logo (which is equivalent to the Boolean cube representation of logically-reversible OR gate), our proposed valleytronic-based reversible logic gate encodes information in the valley polarization of the computation output. This allows reversible circuits to be constructed with significantly reduced wasteful bits. This valleytronic-based approach may provide a new route towards reversible computing, which has broad applications including cryptography, signal and graphic processing, quantum computation, and is ultimately required to improve the energy efficiency of classical computer beyond the Landauer's limit – a lower bound of waste-heat generation due to logically-irreversible computation. This work was awarded first prize in the FIRST Industry Workshop 2017.

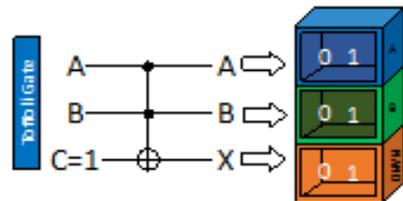
Y. S. Ang, S. A. Yang, C. Zhang, Z. Ma, L. K. Ang, 'Valleytronics in merging Dirac cones: All-electric-controlled valley filter, valve and universal reversible logic gate', *Physical Review B*, in press (2017).



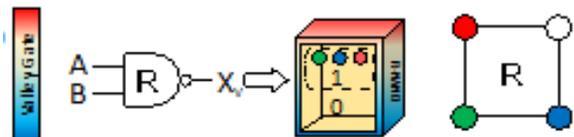
EPD



Valleytronic-based reversible OR gate



Traditional reversible logic gate



Valleytronic reversible logic gate